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10/729,196	12/05/2003	Gary L. Swoboda	TI-34670	8832

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EXAMINER	
ELPENORD, CANDAL	
ART UNIT	**PAPER NUMBER**
2616	

NOTIFICATION DATE	DELIVERY MODE
11/29/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/729,196	SWOBODA ET AL.	
	Examiner	Art Unit	
	Candal Elpenord	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *2-3, 6, 10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-5, 7-9* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The indicated allowability of claims 3 and 6 are withdrawn in view of the newly discovered reference(s) to Huang et al (US 7,010,712 B1), Pauw et al (US 2004/0015879 A1), and McCullough et al (US 6,615,371 B2). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 1, 4, 5, 7-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohashi et al. (US 2004/0078690 A1) in view of Huang et al (US 7,010,712 B1) in further view of McCullough et al (US 6,615,371 B2) and Pauw et al (US 2002/0015879 A1).

Regarding claim 1, Kohashi et al. discloses a timing trace stream having a logic signal associated with each clock cycle, the timing trace stream being transmitted in packets groups having a plurality of packets a method of compressing the timing trace stream, the method comprising: wherein each group of packets (fig. 14, plurality of packets, recited in paragraph 0008) has at least one header (fig. 14, "header packet", recited in paragraph 0008) packet and at least one information packet (fig. 14, "packet data", recited in paragraph 0008), **regarding claim 4**, Kohashi et al. discloses the method ("program counter trace", recited in abstract, lines 1-6) further comprising: representing an activity ("operating and stopping", recited in paragraph 0050 and "status indicating operating", recited in paragraph 0051, lines 5-15) of the a program counter (fig. 1 and fig. 3, Program Counter 116, recited in paragraph 0049) with a first logic signal during a clock cycle (fig. 1, Processor Clock 101 as the operation clock, recited in paragraph 0050); and representing a non-activity ("stopping ", recited in paragraph 0050 and paragraph 0051, lines 5-15) of the program counter (fig. 1 and fig.

3, Program Counter 116, recited in paragraph 0049) with a second logic signal (fig. 1, Processor Clock 101 as the operation clock, recited in paragraph 0050); **regarding claim 5**, an apparatus (fig. 1, Program Counter Trace System, recited in paragraphs 0049-0051, recited in paragraph 0051 and abstract, lines 1-6) for generating a timing trace stream in a target processor (fig. 1, Debugger 122, recited in paragraph 0053, lines 1-7) a logic signal ("each clock cycle", recited in paragraph 0055, lines 1-6) being associated with each target processor clock cycle (fig. 1, Processor Clock 101, recited in paragraph 0050), the apparatus (fig. 1, Trace Clock Generating Unit, recited in paragraph 0051, lines 5-15) comprising: a logic unit (fig. 2, Logic Unit 213, recited in paragraph 0055, lines 17-19) responsive to a preselected number of logic signals (fig. 1, Processor Clock 101, recited in paragraph 0050), the logic unit providing a first control signal when all of the preselected logic signals are different, the logic signal providing a second control signal when all the preselected logic signals are the same; a first storage unit (fig. 8, Trace FIFO 1-802, recited in paragraph 0076, lines 1-6) responsive to the preselected logic signals for storing the each logic signal ("storing of signal numbers", recited in paragraph 0074) in a predetermined storage location (fig. 9, Trace FIFO 1, 32bit, recited in paragraph 0074), the first storage unit responsive to the first control signal (fig. 8, FIFO Control Unit 1, recited in paragraph 0073, lines 9-11) for transferring the contents ("transferring the parallel data stored in second trace FIFO in accordance with instruction", recited in paragraph 0073, lines 7-22) of then the first storage unit (fig. 8, Trace FIFO 1-802, recited in paragraph 0076, lines 1-6); a second storage unit (fig. 8, Trace FIFO 2-805, recited in paragraph 0076, lines 6-20)

responsive to preselected logic signals for storing the current logic signal ("state storage and signal numbers of trace", recited in paragraph 0074) in a preestablished storage unit location (fig. 10, Trace FIFO 2, recited in paragraph 0074), the second storage unit (fig. 8, Trace FIFO 2-805, recited in paragraph 0076, lines 6-20) storing a signal group ("signal numbers", recited in paragraph 0074) representing a multiple of the preselected number the second storage unit (fig. 8, Trace FIFO 2-805, recited in paragraph 0076, lines 6-20) responsive to the second logic signal (fig. 8, FIFO Control Unit 2, recited in paragraph 0073, lines 11-15) for transferring the contents ("transferring the parallel data stored in second trace FIFO in accordance with instruction", recited in paragraph 0073, lines 7-22) of the second storage unit (unit (fig. 8, Trace FIFO 2-805, recited in paragraph 0076, lines 6-20), **regarding claim 7**, the apparatus (fig. 1,Device 110, recited in paragraphs 0051-0050), wherein each of the preselected number of logic signals (fig. 1, Trace clock Generation Unit 108 and trace clock 111, recited in paragraph 0051, lines 5-15) representing an activity (fig. 3, "trace status of the PC", recited in paragraph 0056, lines 1-13) of a program counter (fig. 1 and fig. 3, Program Counter 116, recited in paragraph 0049) during an associated clock cycle ("each cycle of processor clock", recited in paragraph 0056, lines 1-13), **regarding claim 8**, the apparatus (fig. 1,Device 110, recited in paragraphs 0051-0050) further comprising a first in/first out storage unit (fig. 6, Trace FIFO, recited in paragraph 0067, lines 14-30), the contents ("parallel selected data", recited in paragraph 0067, lines 14-30) of the first and the second storage unit being transferred to the first in/first out storage unit ("transferring parallel data stored in FIFO).

Kohashi et al. discloses all the claimed limitation with exception of the following features: regarding claim 1, when a preselected number of clock cycles have at least one logic 1 signal and at least one logic 0 signal associated with each clock cycle, transmitting a standard group of packets having logic signal associated with each of the preselected number of clock cycles; when the preselected number of clock cycles has only one of the logic 1, and the logic 0 signals associated with each clock cycle, transmitting a compressed group of packets, the packets, the packets including an indicia of the one logic signal, the packets including a signal group representing the preselected number.

However, Huang et al. in a similar field of endeavor discloses the following features: regarding claim 1, when a preselected number of clock cycles (fig. 2 and fig. 3 for series of logic ones and zeroes) have at least one logic 1 signal and at least one logic 0 signal (fig. 3 and fig. 2, logic ones and zeroes, recited in col. 3, lines 29-49) associated with each clock cycle ("clock signal", recited in col. 3, lines 29-49), transmitting a standard group of packets ("outputting a serial data stream", recited in col. 3, lines 29-49) having logic signal (fig. 3, CLKI signals) associated with each of the preselected number of clock cycles (fig. 2 and fig.3, CLKI signals, recited in col. 3, lines 29-49); when the preselected number of clock cycles (fig. 2 and fig.3, CLKI signals, recited in col. 3, lines 29-49) has only one of the logic 1, and the logic 0 signals (fig. 3, CLKI logic signals) associated with each clock cycle ("clock signal", recited in col. 3, lines 29-49), transmitting a compressed group of packets (" outputting a serial data stream which includes a series of data frames", recited in col. 3, lines 29-49) the

packets ("data frames", recited in col. 3, lines 29-49) including an indicia ("pulses of serial data frame", recited in col. 4, lines 66-67 and col. 5, lines 1-7) of the one logic signal (fig. 2, and fig. 3, clock diagram, the packets ("data frames", recited in col. 3, lines 29-49) including a signal group ("framing signal", recited in col. 3, lines 29-49) representing the preselected number (fig. 2 and fig. 3 for plurality of logic signals). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Kohashi et al. by using features as taught by Huang et al. in order to synchronization of serial data stream output from a multiple port system (See col. 2, lines 20-29 for motivation).

Kohashi et al and Huang et al. disclose all the subject matter of the claimed invention with exception of being silent with regard to the following features: **regarding claim 1**, wherein the standard group of packets includes a plurality of information packets and the compressed group of packets includes one in formation packet., **regarding claim 5**, wherein the storage location in the first and the second storage units are arranged in groups of packets, each group of packets including control signals.

However, McCullough et al (US 6,615,371 B2) in a similar filed of endeavor discloses the following features: **regarding claim 1**, wherein the standard group of packets (fig. 6, Meaning full data of Trace, recited in col. 5, lines 7-14) includes a plurality of information packets ("status bits of pipe information", recited in col. 5, lines 15-49) and the compressed group of packets ("compressible packets", recited in col. 6, lines 9-28) and bits of data in trace stream", recited in col. 5, lines 41-67) includes one

information packet ("pipe status information bits", recited in col. 5, lines 41-67), **regarding claim 5**, wherein the storage location (fig. 2, RAM 17, recited in col. 4, lines 14-20) in the first and the second storage units ("compressible packets and send to trace port RAM", recited in col. 6, lines 9-28) are arranged in groups of packets, each group of packets including control signals ("group of substantive signals", recited in col. 5, lines 42-56) with the packet payload ("bits of data in trace packets", recited in col. 5, lines 42-56). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Kohashi et al. by using features as taught by McCullough et al. in order to record and transferring viewable trace data (See col. 2, lines 22-47 for motivation).

Kohashi, Huang, and McCullough disclose all the claimed limitation with the exception of being silent with respect to the following features:, **regarding claim 5**, the logic unit providing a first control signal when all of the preselected logic signals are different, the logic signal providing a second control signal when all the preselected logic signals are the same.

However, Pauw et al. in a similar field of endeavor discloses the logic unit (fig. 1, Processor 2, Trace Mechanism 100, and time interval, recited in paragraph 0015) providing a first control signal (fig. 1, enable/disable and control of task and details, recited in paragraph 0015) when all of the preselected logic signals are different (fig. 2, list of events, recited in paragraph 0023, the logic signal unit (fig. 1, Processor 2, Trace Mechanism 100 and time interval, recited in paragraph 0015) providing a second control signal (fig. 1, enable/disable and control of task and details, recited in

paragraph 0015 when all the preselected logic signals are the same(fig. 1, enable/disable and control of task and details, recited in paragraph 0015 and paragraph 0026-0027). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Kohashi et al. with Huang, and McCullough by using features as taught by Pauw et al. in order to analyze program tasks at different time intervals (See paragraph 0007-0008 for motivation).

6. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kohashi et al (US 2004/0078690 A1) in view of Huang et al (US 7,010,712 B1) in further view of Swaine et al (US 7,003,699 B2).

Regarding claim 9, Kohashi et al. discloses a system ("program counter trace system", recited in abstract, lines 1-6), for transferring data concerning the operation of target processor (fig. 1, Processor 110, recited in paragraphs 0049-0051) to a host processing unit (fig. 1, Personal Computer 121/Debugger 122, recited in paragraph 0053) the system ("program counter trace system", recited in abstract, lines 1-6) comprising: a program counter trace stream generation unit (fig. 1, Trace Flag Generation Unit 104, recited in paragraph 0051), the program counter trace stream generation unit (fig. 1, Trace Flag Generation Unit 104, recited in paragraph 0051) generating a trace stream (fig. 1, "trace serial data 112", recited in paragraph 0052, lines 1-8) identifying each activity ("operating and stopping", recited in paragraph 0050 and "status indicating operating", recited in paragraph 0051, lines 5-15) of the program

counter (fig. 1 and fig. 3, Program Counter 116, recited in paragraph 0049), and a timing trace stream generation unit (fig. 1, Trace Clock Generating Unit 108, recited in paragraph 0051, lines 5-15) the timing trace stream generation unit (fig. 1, Trace Clock Generating Unit 108, recited in paragraph 0051, lines 5-15) generating a timing trace stream (fig. 1, Trace Clock 11, recited in paragraph 0052, lines 1-9), a first logical signal ("each clock cycle", recited in paragraph 0055, lines 1-6) identifying when the program counter performed an activity ("operating", recited in paragraph 0051, lines 12-15 and "operating", recited in paragraph 0050) during the associated clock cycle ("each cycle of processor clock", recited in paragraph 0056, lines 1-13) and a second logic signal ("each clock cycle", recited in paragraph 0055, lines 1-6) identifying when the program counter was non-active ("stopping", recited in paragraph 0050) during an associated clock cycle ("each cycle of processor clock", recited in paragraph 0056, lines 1-13).

Kohashi et al. discloses all the claimed limitation with the exception of being silent in regard to the following features: **regarding claim 9**, a timing trace stream having a first mode of operation generating a timing trace header packet and a first information packet stream with a logical signal associated each clock cycle.

However, Huang et al (US 7,010,712) in a similar field of endeavor discloses a timing trace stream ("timing device", recited in col. 3, lines 29-49) having a first mode of operation ("generating of serial data stream up receiving a clock signal as the first mode, recited in col. 3, lines 29-49) generating a timing trace header packet ("data frame with status information", recited in col. 3, lines 29-49) and a first information

packet stream ("generating serial data stream with data frames at a specific time", recited in col. 3, lines 29-49) with a logical signal (fig. 2, CLKI 24, recited in col. 3, lines 29-32) associated each clock cycle (fig. 2, CLKI 24, recited in col. 3, lines 29-32), the timing trace stream generation unit ("timing device", recited in col. 3, lines 29-49) having a second mode of operation (fig. 3, Reset Signal 26, recited in col. 3, lines 58-67) generating a header packet ("data frame with status information", recited in col. 3, lines 29-49) and a second timing trace information packet ("serial data unit", recited in col. 3, lines 29-49), the second timing trace information packet replacing ("reset signal and generating a serial data stream", recited in col. 3, lines 29-49 and fig. 4, Supply Reset Signal 100, recited in col. 4, lines 43-67) at least one first information packet ("data frame with status information", recited in col. 3, lines 29-49) when all of the logic signals ("common clock signal", recited in col. 3, lines 29-37) in the at least one first information packet ("data frame with status information", recited in col. 3, lines 29-49) are the same logic signal ("common clock signal", recited in col. 3, lines 29-30). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Kohashi et al. by using features as taught by Huang et al. in order to provide synchronization of serial data stream output from a multiple port system (See col. 2, lines 20-29 for motivation).

Kohashi et al. and Huang et al. disclose all the subject matter of the claimed invention with the exception of being silent with regard to the following features: the timing trace generation unit including a logic unit, the logic unit generating control

signals determining whether the first information packet stream or the second information packet is transferred to the host processing unit.

However, Swaine et al. in a similar field of endeavor discloses the timing trace generation unit (fig. 1, ON-Chip Trace Module, recited in col. 8, lines 17-27, fig. 2, Trace Generation Block 120, recited in col. 8, lines 58-67 and col. 9, lines 1-2) including a logic unit (fig. 4, Funnel Logic 460, recited in col. 12, lines 1-7) the logic unit (fig. 4, Funnel Logic 460, recited in col. 12, lines 1-7) generating control signals ("the logic unit arranged to issue control signals", recited in col. 5, lines 28-32) determining whether the first information packet stream ("trace stream signal", recited in col. 4, lines 43-62) is transferred ("outputting trace signals", recited in col. 4, lines 43-62) to the host processing unit ("processing apparatus", recited in abstract, lines 1-8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Kohashi et al. with Huang et al. by using features as taught by Swaine et al. in order to classify the trace signals generating by the trace generation unit (See col. 2, lines 22-47 for motivation).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Washington et al (US 5,920,572), Yamamoto et al (US 6,961,872 B2), and Hayase et al (US 2003/0192034 A1) are cited to show methods and system related to claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Candal Elpenord whose telephone number is (571) 270-3123. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Bin Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CE

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SUPERVISORY PATENT EXAMINER